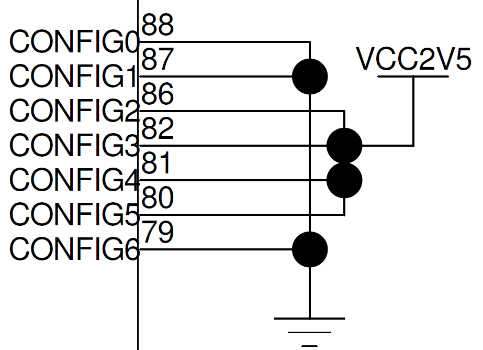
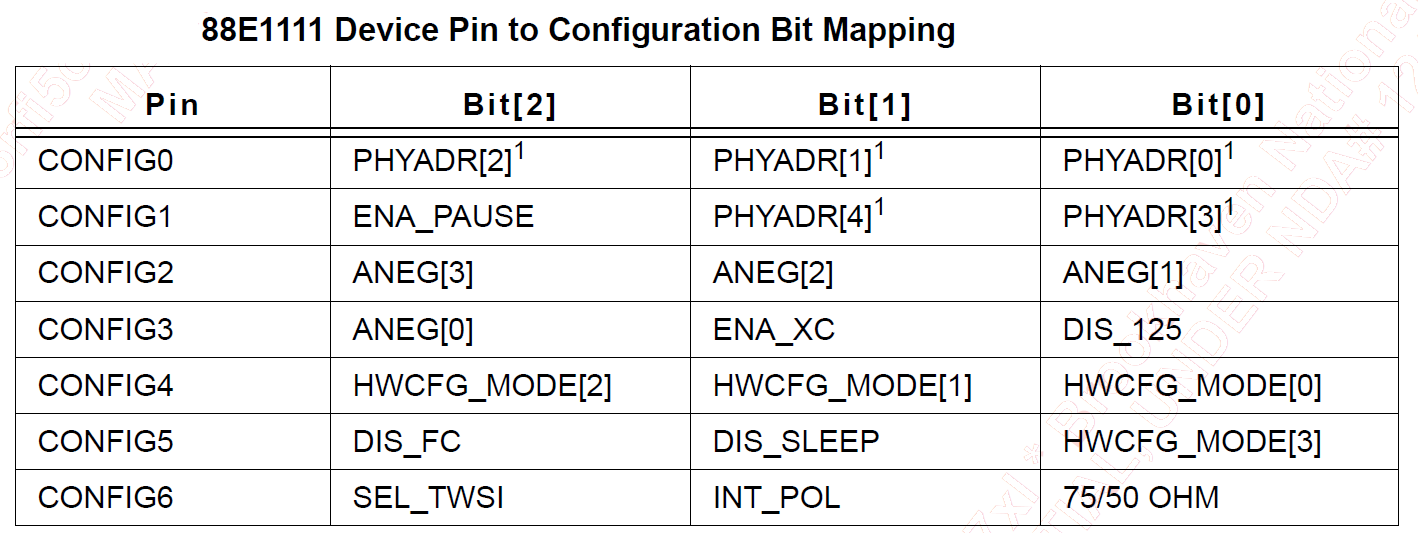
# Network Design

The Ethernet connection of Pizzabox is built on a Marvell 88E1111 PHY device.

## **Hardware Configuration:**





|  |  |  |
| --- | --- | --- |
| PIN | Value | Parameter |
| CONFIG0 | 0 | PHYADR[2:0] = 111 |
| CONFIG1 | 0 | ENA\_PAUSE = 1; PHYADR[4:3] = 11 |
| CONFIG2 | 1 | ANEG[3:1] = 111 |
| CONFIG3 | 1 | ANEG[0] = 1; ENA\_XC = 1; DIS\_125 = 1 |
| CONFIG4 | 1 | HWCFG\_MODE[2:0] = 111 |
| CONFIG5 | 1 | DIS\_FC = 1; DIS\_SLEEP = 1; HWCFG\_MODE[3] = 1 |
| CONFIG6 | 0 | SEL\_TWSI = 0; INT\_POL = 0; 75/50 OHM = 0 |

* PHYADR[4:0] = 00000
* Enable Pause: default register 4.11:10 to 00
* Auto-negotiation enabled, advertise all capabilities, prefer Slave
* Enable crossover.
* Disable 125MHz clock.
* GMII/MII to copper
* Disable fiber/copper interface autoseelection.
* Disable energy detect.
* Select MDC/MDIO interface.
* INTn signal is active HIGH.
* 50 OHM termination.

## **MDIO interface**



## MDIO Packet Format

|  |  |
| --- | --- |
|  |  |
| PRE\_32 | 32-bits of '1' |
| ST | 2-bits of '01' |
| OP | 2-bits of Opcode |
| PA5 | 5-bits of PHY address |
| RA5 | 5-bits of register address |
| TA | 2-bits of turn-around |
| D16 | 16-bits of data (sent by either SME or PHY, depending on OP) |
| Z | tristate MDIO |

When the MAC drives the MDIO line, it has to guarantee a stable value 10 ns (setup time) before the rising edge of the clock MDC. Further, MDIO has to remain stable 10 ns (hold time) after the rising edge of MDC.

When the PHY drives the MDIO line, the PHY has to provide the MDIO signal between 0 and 300 ns after the rising edge of the clock.[[1]](https://en.wikipedia.org/wiki/Management_Data_Input/Output#cite_note-1) Hence, with a minimum clock period of 400 ns (2.5 MHz maximum clock rate) the MAC can safely sample MDIO during the second half of the low cycle of the clock..

MDC frequency: to be checked for 88E1111.